Claims 1-4, 41, 46-48, 50, 58, 60-61, 79, 81, 83, 89, 90 and 92 have been amended.

The claims have been amended to clarify language used in the claims. The amendments are intended to merely clarify the claims, and the scope of the claims is intended to be the same after the amendment as it was before the amendment. No new matter is added with the amendments.

The Examiner's allowance of Claims 72-78 is acknowledged.

Objections to claims.

The Examiner objected to Claims 92 and 41 for informalities. Claim 92 has been amended as suggested by the Examiner. Claim 41 has been amended to recite "*the step* of annealing."

Rejections under 35 U.S.C. § 112(2).

The Examiner rejected Claims 3, 4 and 79 under Section 112(2) as indefinite.

Claims 3 and 4 have been amended to eliminate the term "silicon" and recite the term "the substrate."

Claim 79 has been amended to recite "*a* horizontal surface."

Accordingly, it is respectfully submitted that the claims as amended fully comply with Section 112(2), and withdrawal of this rejection is respectfully requested.

Rejection under 35 U.S.C. §102(b) (Witek)

The Examiner rejected Claim 47 as anticipated under Section 102(b) by USP 5,393,681 (Witek). This rejection is respectfully traversed.

The basis of the Examiner's rejection is that Witek discloses a method of forming a vertical structure on a substrate as recited in Claim 47, referring to Figure 32.

Witek does not describe or suggest forming a vertical structure having multiple overlying epitaxial layers such that *insulative spacers are formed over the sidewalls of each epitaxial layer.*

Witek discloses forming vertically raised transistors by forming overlying layers of a dielectric layer 102, a conductive layer 104, a dielectric layer 106, a conductive layer 108, and a dielectric layer 110. Sidewall dielectric layers 116, 118 are formed *onto the conductive layers*

104, 108. Regions 120, 122, 124 are then epitaxially grown *adjacent to* the sidewall layers 116, 118 and dielectric layers 102, 106, 110.

Witek describes the process at col. 12, lines 52-68, as follows (emphasis added):

> *In FIG. 31, a sidewall dielectric layer 116* ***is formed adjacent*** *the sidewall of the conductive layer 104 and a sidewall dielectric layer 118* ***is formed adjacent*** *the sidewall of the conductive layer 108 as taught herein. A region 120 is epitaxially grown* or selectively formed from the surface of the substrate 100 or from a surface of the diffusion 112 if the diffusion 112 is formed. Region 120 is of a first conductivity type which is either N-type or P-type. *A region 122 is epitaxially or selectively formed overlying the region 120.* The region 122 is of a second conductivity type wherein the second conductivity type is opposite the first conductivity type. ***Region 122 is formed laterally adjacent the sidewall dielectric layer 116.*** *An epitaxial step or selective formation step is used to form region 124* which is of the first conductivity type. ***The region 124 lies partially adjacent the sidewall dielectric layer 118...***

This is clearly depicted in FIG. 32, cited by the Examiner:

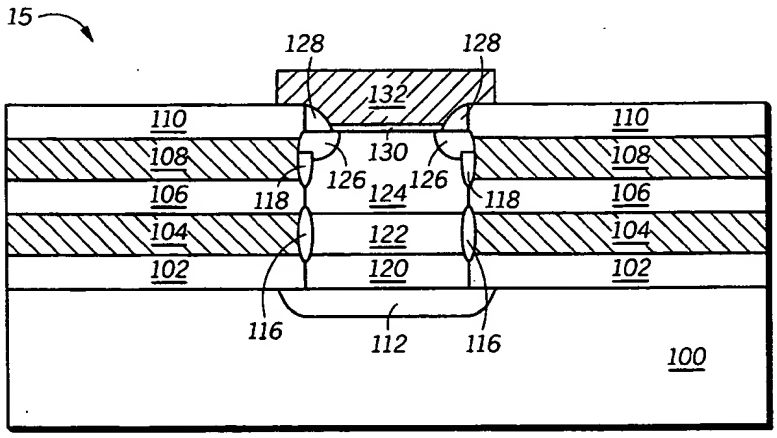

FIG. 32

As shown and described, the dielectric layers 116, 118 are formed prior to and not as part of the epitaxially grown layers. By comparison, Applicant's method as recited in Claim 47 comprises forming multiple overlying epitaxial layers such that each epitaxial layer comprises *insulative spacers formed over the sidewalls of the epitaxial layers.*

Accordingly, Witek does not teach or suggest Applicant's method as recited in Claim 47, and withdrawal of this rejection is respectfully requested.

Rejection under 35 U.S.C. §102(e) and §103(a) (Nakamura)

The Examiner rejected Claims 1, 8, 32, 33, 35, 44 and 45 as anticipated under Section 102(e) by USP 6,391,692 (Nakamura). The Examiner rejected depending Claims 2, 24, 25, 34, 38, 39, 50, 52, 53, 61and 68 under Section 103(a) as obvious over Nakamura. These rejections are respectfully traversed.

Nakamura describes the manufacture of a transistor that includes an elevated source/drain structure made by selective epitaxial growth. The stated object of Nakamura is to provide a construction such that *when the source/drain structure (51) is formed by selective epitaxial growth under heat*, silicon atoms of the underlying silicon layer (43) do not migrate and aggregate adjacent the structure (51) to break down its shape. See Abstract, col. 2 at lines 1-7 and 9-12, and col. 5, lines 39-44:

Nakamura describes the method as follows (col. 2, lines 23-34, emphasis added):

> Further, there is provided a method of manufacturing a field effect transistor, according to the present invention, which comprises preparing a substrate on which a first semiconductor layer, a first insulating layer *and a second semiconductor layer are stacked in order*, forming an element isolation layer within the second semiconductor layer, forming a gate electrode over the substrate with a gate insulating film interposed therebetween, forming a second insulating layer so as to cover angular portions on the main surface side of an activation layer defined by the element isolation layer, *and forming a third semiconductor layer by a selective epitaxial growth method with the gate electrode and the second insulating film as masks.*

See also col. 4, line 51 to col. 5, line 38, describing the process with reference to FIG. 5.

Nakamura describes *stacking* a silicon layer (41), an insulating layer (42), and a silicon layer (43) to form an SOI substrate (40), and forming a single silicon layer (51) by selective epitaxial growth to form an elevated source/drain structure.

Nakamura does not teach or suggest Applicant's method of selectively growing a first epitaxial layer, forming an insulative layer onto epitaxial layer, removing a portion of the insulative layer; selectively growing a second epitaxial layer, and forming an insulative layer thereover. Nor does the disclosure of Nakamura make obvious Claims 2, 24, 25, 34, 38, 39, which depend either directly or indirectly from Claim 1, or Claims 50, 52, 53, 61and 68.

Accordingly, withdrawal of these rejections is respectfully requested.

Rejection under 35 U.S.C. §102(b) and §103(a) (Mazuré)

The Examiner rejected Claims 83-85, 88-91, 93, 95, 97 and 99 as anticipated under Section 102(b) by USP 5,308,782 (Mazuré). The Examiner also rejected Claims 86, 87, 92, 94, 97, 98 and 100 under Section 103(a) as obvious over Mazuré. These rejections are respectfully traversed.

The Examiner maintains that Mazuré teaches Applicant's methods of forming an elevated transistor, with reference to Mazuré at FIGS. 15-20.

Mazuré describes forming a vertically stacked transistor structure at col. 8, line 56 to col. 10, line 31. According to Mazuré's method, conductive layers 60, 64, and 68 and dielectric layer 58, 62, 66, and 70 are formed overlying a substrate 12. An opening is etched through the conductive and dielectric layers. The sidewalls of the conductive layers 60, 64, and 68 are over-etched to form recesses. A dielectric material is then deposited to form a dielectric layer 74 and laterally recessed *sidewall dielectric layers 72* on the sidewalls of the conductive layers 60, 64, 68 (col. 9, lines 18-21).

This is illustrated in FIG. 16 below.

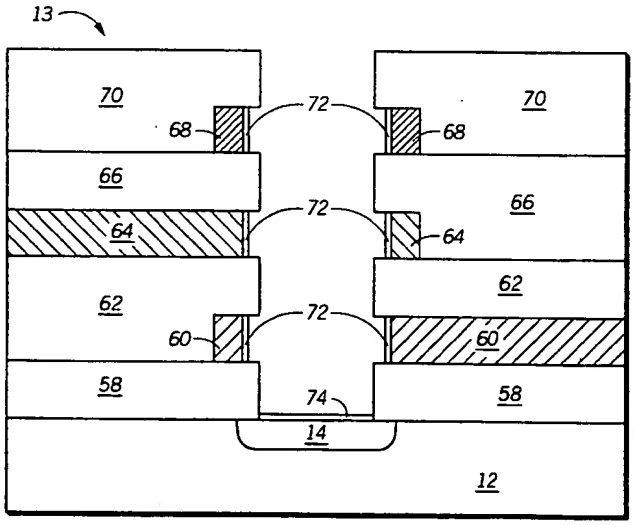

FIG.16

Stacked transistors are then formed in the opening, as illustrated in FIG. 17.

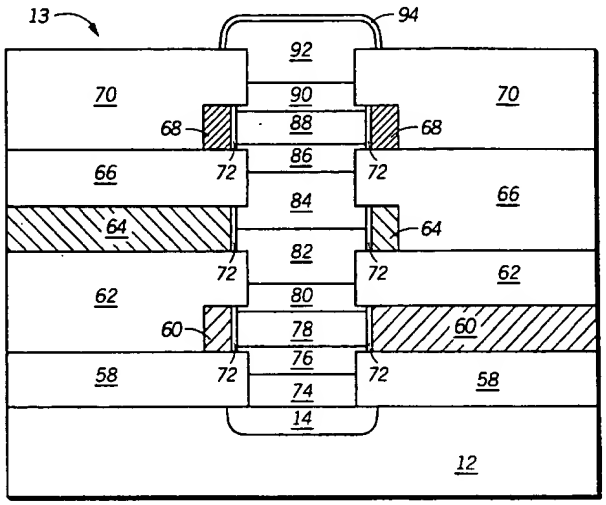

FIG.17

In FIG. 17, a first and a second transistor are formed one on top of the other. The first transistor includes a first electrode which has a lightly doped region 76 and a heavily doped region 74, a channel region 78,and a second electrode which has a lightly doped region 80 and a heavily doped region 82. The second transistor includes a first electrode which has a lightly doped region 86 and a heavily doped region 84, a channel region 88, and a second electrode which has a lightly doped region 90 and a heavily doped region 92.

With reference to FIG. 4, Mazuré describes a method of forming the electrodes and channel regions within the device opening by epitaxial growth. See col. 4, line 26 to col. 5, line 13.

> In FIG. 4, first and second current electrodes, also respectively referred to as a drain and a source, and a channel region are formed...
>
> Initially, a first current electrode or drain electrode 28 is formed in the device opening...***Drain electrode 28 is grown adjacent the first dielectric layer 16****, with in-situ doping, until the drain electrode 28 is adjacent or nearly adjacent a bottom portion of the sidewall dielectric 22 as illustrated in FIG. 4. ..*
>
> ***Epitaxial growth continues*** in a similar manner to form a channel region 30...The channel region is grown, with in-situ doping, *until the electrode is adjacent or nearly adjacent a top portion of the sidewall dielectric 22* as illustrated in FIG. 4.
>
> *Epitaxial growth continues* in a similar manner to form a second current electrode, also referred to as a source electrode, of a second conductivity type. The second current electrode has two sub-regions. The two sub-regions are a lightly doped electrode 32 and a heavily doped electrode 34. The electrodes 32 and 34 are formed by changing the in-situ doping concentration during growth. Initially, the second conductivity doping gas is at a

> predetermined concentration. After a predetermined time, and therefore after a predetermined epitaxial growth thickness, the lightly doped electrode 32 is formed and the dopant concentration is increased to a second predetermined level. While maintaining the second predetermined level, *epitaxial growth continues* to form the heavily doped electrode 34.

Contrary to Applicant's method, Mazuré teaches a *continuous* process to form the conductive regions by epitaxial growth. In addition, the regions are formed *adjacent to* the dielectric layer 58, 62, 66, and 70 and the previously formed sidewall spacers 72.

Mazuré does not teach or suggest Applicant's method as recited in Claim 83 of forming a first epitaxial layer over a buried drain, forming an insulative layer over the epitaxial layer, removing a portion of the insulative layer; forming a second epitaxial layer, and forming an insulative layer thereover. Nor does Mazuré teach or suggest Applicant's method as recited in Claim 89 of forming an elevated transistor by forming an elevated gate over a buried drain, the gate comprising multiple overlying epitaxial layers in a vertical orientation with each epitaxial layer comprising sidewalls and an upper surface, *and insulative spacers formed on the sidewalls.*

Nor does the disclosure of Mazuré make obvious Claims 86 or 87, which depend indirectly from Claim 83, or Claims 91, 94, 97, 98 and 100, which depend directly or indirectly from Claim 89.

Accordingly, Mazuré does not teach or suggest Applicant's method as claimed, and withdrawal of this rejection is respectfully requested.

Rejection of Claims under 35 U.S.C. 103(a) (Ma as primary reference)

The Examiner rejected Claims 1-8, 27-32, 35-37, 40-44, 46, 48-51, 54-63, 69-71 and 79-82 under Section 103(a) as obvious over U.S. Patent No. 5,998,248 (Ma). The Examiner also rejected Claims 9-23, 26, 61, and 64-67 under Section 103(a) as obvious over Ma in view of U.S. Patent No. 6,319,782 (Nakabayashi). These rejections are respectfully traversed.

The Examiner admits that Ma lacks anticipation on forming a layer of an insulative material over the second epitaxial layer, and repeating the steps of removing a portion of the insulative layer, growing an epitaxial layer and forming an insulative layer to provide a vertical structure of a desired height. However, the Examiner maintains that Ma suggests "subjecting the device to conventional processing to provide a finished device," referring to col. 4, lines 5-7, so that it would be obvious to form a layer of insulative material over the second epitaxial layer "to provide conventional device insulation." The Examiner further maintains that it would be

obvious to repeat the method steps "since it is conventionally performed in the art in order to obtain a device of a desire[d] height."

Ma describes a method of fabricating ultrashallow junctions with desired separation and isolation between source/drain regions and gate regions.

There is no motivation based on Ma's teaching to deposit a layer of insulative material over the second epitaxial layer (11). The purpose of forming the insulating layer 9 over the silicon layer 7 is to create a taper-shaped isolation where the source and drain regions (8) meet the gate regions (3). The isolation layer (9) is formed to reduce capacitance and to ensure a narrow separation and insulation between the source/drain regions 8 and the gate conductor 3. This is illustrated in FIG. 5.

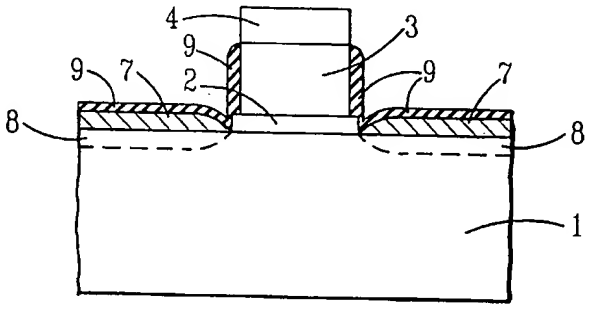

FIG. 5

Ma then covers a portion of the insulating layer (9) with an insulating spacer (10), removes a portion of the insulating layer (9), and forms a second epitaxial silicon layer (11).

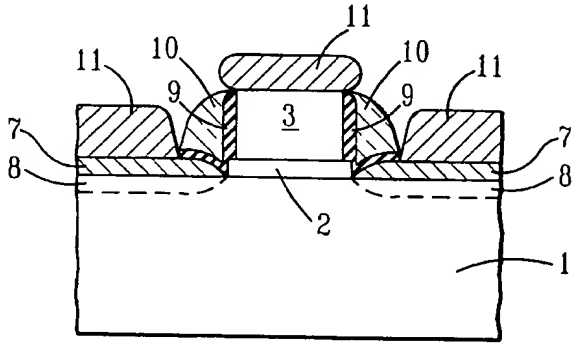

FIG. 6

One would not be motivated to form a further isolation layer (9) over the second epitaxial layer (11) since such an isolation layer would not be needed for separation and insulation of the source/drain regions, as taught by Ma.

Furthermore, Ma teaches depositing a silicide-forming metal (W, Ti, Co, Ni) on the *exposed* silicon surface (11) to silicide the top surfaces of the source and drain regions and polysilicon gate regions, as illustrated in FIG. 7.

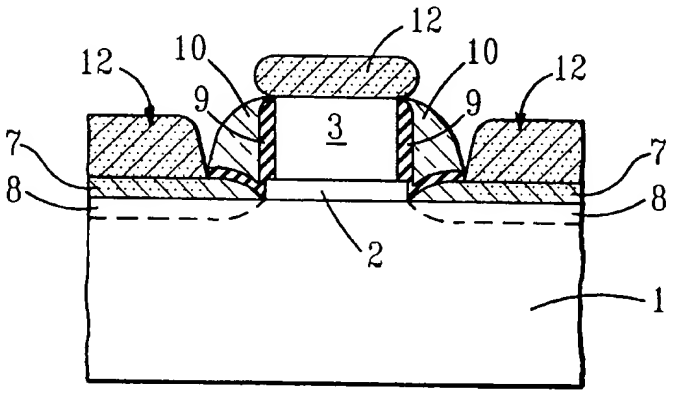

FIG. 7

Ma teaches that the metal silicide (12) reduces the resistivity in the gate conductor (col. 1 at lines 47-48, and cols. 3-4, bridging paragraph.) Formation of an insulating layer over the silicon surface (11) would be counter to that process step and Ma's invention.

There is no motivation based on Ma's disclosure to form an insulating layer over the second epitaxial layer 11.

In addition, Ma does not disclose "subjecting the device to conventional processing to provide a finished device" as the Examiner contends. At col. 4, lines 5-7, Ma discloses:

> If desired, the device can then be subjected to conventional processing **in order to form contacts and wiring** to provide the desired finished device.

This passage in Ma does not teach or suggest forming an insulative layer on a second epitaxial layer.

Further, the Examiner's statement that the steps of forming a layer of an insulative material over the second epitaxial layer, and repeating the steps of removing a portion of the

insulative layer, growing an epitaxial layer and forming an insulative layer to provide a vertical structure of a desired height are "conventionally performed in the art" is without basis and merely the Examiner's unsupported opinion. Applicant fails to find any basis for this statement in Ma or in any of the cited references.

Ma does not teach or suggest Applicant's method of selectively growing a first epitaxial layer, forming an insulative layer onto epitaxial layer, removing a portion of the insulative layer; selectively growing a second epitaxial layer, and forming an insulative layer thereover, as claimed by Applicant. Accordingly, withdrawal of this rejection is respectfully requested.

As for the rejection of Claims 9-23, 26, 61, and 64-67, the Examiner maintains that it would be obvious to form the silicon layers in Ma by using the processing ranges, parameters, gases and dopants disclosed in Nakabayashi to arrive at Applicant's method as claimed.

The mere disclosure in Nakabayashi of various processing parameters does not overcome the deficiencies of Ma to obviate Applicant's method as claimed.

Nothing in the disclosure of Ma, either alone or combined with Nakabayashi, teaches or suggests Applicant's method as claimed. Accordingly, withdrawal of these rejections of the claims is respectfully requested.

Cited Prior Art. The prior art made of record and not relied upon is acknowledged. Nothing in those references teaches or suggests Applicant's method as claimed.

Extension of Term. The proceedings herein are for a patent application and the provisions of 37 CFR § 1.136 apply. Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that Applicant has inadvertently overlooked the need for a petition for extension of time. If any extension and/or fee are required, please charge Account No. 23-2053.

Based on the above remarks, the Examiner is respectfully requested to reconsider and withdraw the rejections of the claims. It is submitted that the present claims are in condition for allowance, and notification to that effect is respectfully requested.

Respectfully submitted,

Kristine M Strodthoff

Dated: September 19, 2002

Kristine M. Strodthoff
Registration No. 34,259

P.O. ADDRESS:

WHYTE HIRSCHBOECK DUDEK S.C.
111 East Wisconsin Avenue, Suite 2100
Milwaukee, Wisconsin 53202
(414) 273-2100

Customer No. 31870

Blacklined Claims

WHAT IS CLAIMED IS:

1. (amended) A method of forming a vertical structure on a substrate, comprising the steps of:

selectively growing a first epitaxial layer of monocrystalline silicon on the substrate; the first epitaxial layer comprising sidewalls and a top surface;

forming a layer of an insulative material over the sidewalls and the top surface of the first epitaxial layer;

removing a portion of the insulative layer to form insulative spacers over the sidewalls and expose ~~only a~~the top surface of the first epitaxial layer;

selectively growing a second epitaxial layer of monocrystalline silicon on the exposed surface of the first epitaxial layer, the second epitaxial layer comprising sidewalls and a top surface; and

forming a layer of an insulative material over the sidewalls and the top surface of the second epitaxial layer.

2. (amended) The method of Claim 1, further comprising repeating the steps of removing a portion of the insulative layer, growing an epitaxial layer, and forming the insulative layer, until the vertical structure reaches a desired height; each of the epitaxial layers ~~having insulated~~ comprising insulative spacers over the sidewalls, and an uppermost epitaxial layer of the vertical structure having insulated sidewalls and an insulated top surface.

3. (amended) The method of Claim 1, wherein the~~silicon~~ substrate comprises monocrystalline silicon.

4. (amended) The method of Claim 1, wherein the~~silicon~~ substrate comprises monocrystalline silicon having a (100) plane orientation.

5. The method of Claim 1, wherein at least one epitaxial layer is grown until a facet having a plane orientation of (100), (110), or (111) is formed on the top surface of the layer.

6. The method of Claim 1, wherein the epitaxial layers are grown until a facet having a plane orientation of (100) is formed on the top surface of the layers.

7. The method of Claim 1, wherein each epitaxial layer has a thickness of up to about 200 nm.

8. The method of Claim 1, wherein one or more epitaxial layers has a thickness of about 70 to about 100 nm.

9. The method of Claim 1, wherein the steps of selectively growing the epitaxial layers comprise introducing a silicon-comprising gas over the substrate.

10. The method of Claim 9, wherein the steps of selectively growing the epitaxial layers comprise:

heating the substrate to about 450°C to about 950°C.; and

flowing at least one silicon-comprising precursor gas over the substrate at a rate of about 10 to about 500 ccm, for about 15 to about 30 seconds.

11. The method of Claim 10, wherein the silicon-comprising gas is flowed over the substrate at a rate and pressure to provide a growth rate of the epitaxial layer at about 20 to about 40 nm/minute.

12. The method of Claim 11, wherein the pressure is about 1 to about 20 Torr.

13. The method of Claim 10, wherein the silicon-comprising gas is flowed over the substrate at a rate and pressure to provide a growth rate of the epitaxial layer at less than about 10 nm/minute.

14. The method of Claim 13, wherein the pressure is about 0.02 to less than about 1 Torr.

15. The method of Claim 13, wherein the pressure is about 0.02 to less than about 1 Torr to provide a growth rate of the epitaxial layer at about 0.3 to less than about 10 nm/minute.

16. The method of Claim 9, wherein the silicon-comprising gas is selected from the group consisting of silane combined with chlorine, disilane combined with chlorine, disilane combined with hydrochloric acid, dichlorosilane, silicon tetrachloride, and combinations thereof.

17. The method of Claim 9, wherein at least one of the steps of selectively growing the epitaxial layer comprises introducing the silicon-comprising gas with a conductivity enhancing dopant.

18. The method of Claim 17, wherein the conductivity enhancing dopant is a p-type dopant.

19. The method of Claim 18, wherein the conductivity enhancing dopant is a p-type dopant selected from the group consisting of diborane, boron trichloride, boron trifluoride, and combinations thereof.

20. The method of Claim 17, wherein the conductivity enhancing dopant is an n-type dopant.

21. The method of Claim 20, wherein the conductivity enhancing dopant is an n-type dopant selected from the group consisting of phosphine, arsine, and combinations thereof.

22. The method of Claim 17, wherein the conductivity enhancing dopant is introduced at a variable rate to provide a concentration gradient of the dopant within the epitaxial layer.

23. The method of Claim 22, wherein the conductivity enhancing dopant is introduced at an increasing rate to provide a low to high concentration of the dopant within the epitaxial layer.

24. The method of Claim 2, further comprising doping the uppermost epitaxial layer by ion implantation.

25. The method of Claim 24, wherein the epitaxial layer is doped using a fluorine-comprising gas selected from the group consisting of PF_3, PF_5, AsF_5, and $B^{11}F_3$.

26. The method of Claim 17, wherein the vertical structure is a source or drain having a height of at least about 10 to about 30 nm.

27. The method of Claim 1, further comprising, prior to the step of selectively growing the first epitaxial film, at least partially removing an oxide layer from the substrate.

28. The method of Claim 27, wherein the step of removing the oxide layer is by an oxide dry etch.

29. The method of Claim 28, wherein the oxide dry etch comprises exposing the substrate to an H_2 gas at about 800°C. to about 850°C.

30. The method of Claim 28, wherein the oxide dry etch comprises exposing the substrate to a reactive plasma at about 100°C.

31. The method of Claim 27, wherein the step of removing the oxide layer is by applying an oxide cleaning solution to the substrate.

32. The method of Claim 1, wherein the insulative layer comprises oxide, nitride, oxidized nitride, or a composite oxide/nitride.

33. The method of Claim 1, wherein the insulative layer comprises silicon nitride.

34. The method of Claim 33, wherein the insulative layer has a thickness of about 5 to about 20 nm.

35. The method of Claim 1, wherein the insulative layer comprises silicon oxide.

36. The method of Claim 35, wherein the insulative layer has a thickness of about 2 to about 5 nm.

37. The method of Claim 1, wherein at least one of the steps of forming the insulative layer is by annealing.

38. The method of Claim 37, wherein the annealing is by rapid thermal nitridation to form a nitride insulative layer.

39. The method of Claim 38, wherein the annealing by rapid thermal nitridation comprises exposing the epitaxial layer to ammonia or nitrogen gas at a pressure of about 100 to about 200 Torr and temperature of about 800°C. to about 1200°C.

40. The method of Claim 37, wherein the annealing is by rapid thermal oxidation to form an oxide insulative layer.

41. (amended) The method of Claim 40, wherein the step of annealing by rapid thermal oxidation comprises exposing the epitaxial layer to a dry oxygen gas at a pressure of about 100 to about 200 Torr and temperature of about 800°C. to about 1200°C.

42. The method of Claim 1, wherein at least one of the steps of removing the insulative layer is by reactive ion etching.

43. The method of Claim 42, wherein the reactive ion etching comprises exposing the insulative layer to an etch gas in an ionized state, the etch gas comprising at least one fluorine-containing gas.

44. The method of Claim 1, wherein the vertical structure is formed adjacent to an existing gate or word line on the substrate.

45. The method of Claim 44, wherein the existing gate or word line is electrically isolated.

46. (amended) A method of forming a raised structure on a substrate, comprising the step of:

forming an epitaxial layer of monocrystalline silicon on the substrate;

forming a layer of insulative material over the epitaxial layer;

removing a portion of the insulative layer to ~~leave only an exposed~~ form insulative spacers over sidewalls and expose a top surface of the epitaxial layer;

forming another epitaxial layer of monocrystalline silicon on the epitaxial layer; and

repeating the steps of forming the insulative layer, removing a portion of the insulative layer, and growing an epitaxial layer, until the vertical structure reaches a desired height, with the uppermost epitaxial layer having an insulated top surface.

47. (amended) A method of forming a vertical structure on a substrate, comprising forming multiple overlying epitaxial ~~layers having insulated~~ layers, each epitaxial layer comprising sidewalls and a top surface, and insulative spacers formed over the sidewalls, and the uppermost epitaxial layer having an insulated top surface.

48. (amended) A method of forming a vertical structure on a substrate, comprising the steps of:

depositing a first epitaxial layer on the substrate, the first epitaxial layer comprising a horizontally oriented surface defining a facet and sidewalls;

forming a layer of an insulative material over the first epitaxial layer;

removing a portion of the insulative layer to expose the horizontal surface and form insulative spacers on the sidewalls of the epitaxial layer;

depositing a second epitaxial layer on the exposed surface of the first epitaxial layer; the second epitaxial layer comprising a horizontally oriented surface defining a facet; and

forming a layer of an insulative material over the second epitaxial layer.

49. The method of Claim 48, further comprising repeating the steps of removing a portion of the insulative layer, growing an epitaxial layer, and forming the insulative layer, until the vertical structure reaches a desired height.

50. (amended) A method of controlling growth of an epitaxial film to form a vertical structure on a substrate, comprising the steps of:

providing a substrate having an elevated structure disposed thereon, the elevated structure having an overlying insulative layer;

forming a first epitaxial layer of monocrystalline silicon on the substrate adjacent to the elevated structure;

forming an insulative layer over the first epitaxial layer;

removing a horizontal surface of the insulative layer to form insulative spacers on sidewalls and expose~~only~~ a top surface of the first epitaxial layer;

forming a second epitaxial layer of monocrystalline silicon over the first epitaxial layer; and

repeating the foregoing steps until the vertical structure is at a desired height.

51. The method of Claim 50, wherein the substrate has an overlying oxide layer, and the method further comprises prior to the step of depositing the first epitaxial layer, removing at least a portion of the oxide layer to expose the substrate.

52. The method of Claim 50, wherein the elevated structure is disposed on an area of microcrystalline silicon that is isolated within the substrate by at least one dielectric isolation region formed in the substrate adjacent thereto.

53. The method of Claim 52, wherein the at least one dielectric isolation region is a shallow trench isolation region comprising an oxide.

54. The method of Claim 50, wherein the vertical structure is a transistor gate.

55. The method of Claim 50, wherein the vertical structure is a source or drain, and at least one of the steps of forming the epitaxial layers is performed with a sufficiently high conductivity doping to effectively dope the source or drain.

56. The method of Claim 55, wherein the elevated structure adjacent to the source or drain is a transistor gate.

57. The method of Claim 55, wherein the vertical structure is a source or drain having a height of about 10 to about 30 nm.

58. (amended) A method of forming an elevated structure on a substrate in a semiconductor processing, comprising the steps of:

providing a semiconductor substrate comprising monocrystalline silicon;

growing a first epitaxial layer on the substrate until a horizontally-oriented facet is formed;

forming an insulative layer over the first epitaxial layer;

removing the insulative layer to form insulative spacers on sidewalls and expose ~~only~~ a horizontal surface of the first epitaxial layer;

growing a second epitaxial layer on the first epitaxial layer until a horizontally-oriented facet is formed; and

repeating the steps of forming the insulative layer, removing a portion of the insulative layer, and growing an epitaxial layer, until the elevated structure is at a desired height.

59. The method of Claim 58, wherein the horizontally-oriented facet of the first and second epitaxial layers has a (100) plane orientation.

60. (amended) A method of forming a raised structure on a silicon substrate, comprising the steps of:

selectively growing a first epitaxial layer of monocrystalline silicon on the substrate;

forming a layer of an insulative material over the first epitaxial layer;

removing the insulative layer to form insulative spacers on sidewalls and expose an upper surface of the first epitaxial layer; and

selectively growing one or more additional epitaxial layers of monocrystalline silicon to form the raised structure to a predetermined height, each epitaxial layer having sidewalls, insulative spacers formed on the sidewalls, and a top surface having the insulative layer removed therefrom, the uppermost epitaxial layer optionally comprising an insulated ~~sidewalls and a~~ top surface.

61. (amended) A method of fabricating an epitaxial structure on a substrate, comprising the steps of:

forming a first epitaxial layer of monocrystalline silicon on the substrate;

annealing the epitaxial layer to form an insulative film thereover;

etching the insulative film to form insulative spacers on sidewalls and expose ~~only~~ a horizontal surface of the first epitaxial layer; and

repeating the foregoing steps to form additional overlying epitaxial layers until a vertical structure having a desired height is reached, the vertical structure comprising multiple epitaxial layers ~~having only insulated~~ comprising spacers formed on the sidewalls, with an uppermost epitaxial layer having insulated sidewalls and an insulated top surface.

62. The method of Claim 61, wherein the step of forming the epitaxial layer comprises heating the substrate and flowing a silicon-comprising gas over the heated substrate.

63. The method of Claim 62, wherein the substrate is heated to about 450°C to about 950°C.

64. The method of Claim 62, wherein the gas is flowed over the substrate to provide a growth rate of the epitaxial layer at about 20 to about 40 nm/minute.

65. The method of Claim 64, wherein the gas is flowed over the substrate at a flow rate of about 10 to about 500 cm, and a pressure of about 1 to about 20 Torr.

66. The method of Claim 62, wherein the gas is flowed over the substrate to provide a growth rate of the epitaxial layer of less than about 10 nm/minute to about 0.3 nm/minute.

67. The method of Claim 66, wherein the gas is flowed over the substrate at a pressure of about 0.02 to less than 1 Torr.

68. The method of Claim 61, wherein the step of annealing is by rapid thermal nitridation to form a nitride insulative layer.

69. The method of Claim 61, wherein the step of annealing is by rapid thermal oxidation to form an oxide insulative layer.

70. The method of Claim 61, wherein the step of etching the insulative layer is by reactive ion etching.

71. The method of Claim 61, wherein each epitaxial layer has a thickness of about 50 to about 200 nm.

72. A method for forming a DRAM cell on a silicon substrate, comprising the steps of:

forming a vertical gate structure on the substrate by the steps of:

forming a first epitaxial layer of monocrystalline silicon on the substrate;

forming a layer of an insulative material over the first epitaxial layer;

removing a portion of the insulative layer to expose only a horizontal surface of the first epitaxial layer; and

repeating the foregoing steps to form one or more additional overlying epitaxial layers until the gate structure is of a desired height, the gate structure comprising multiple overlying epitaxial layers having insulated sidewalls, and an uppermost epitaxial layer having an insulated sidewalls and a horizontal surface; and

forming source and drain regions adjacent to the gate structure.

73. The method of Claim 72, wherein the source and drain regions are elevated.

74. The method of Claim 73, wherein the step of forming the source and drain regions comprises the steps of:

forming while doping, a first epitaxial layer of monocrystalline silicon on the substrate adjacent to the gate structure;

forming a layer of an insulative material over the first epitaxial layer;

removing a portion of the insulative layer to expose only a horizontal surface of the first epitaxial layer;

repeating the foregoing steps to form one or more additional overlying epitaxial layers until the source and drain regions are of a desired height, the source and drain regions comprising multiple overlying epitaxial layers having insulated sidewalls, and an uppermost epitaxial layer having insulated sidewalls and an insulated horizontal surface.

75. The method of Claim 74, wherein the steps of forming the epitaxial layers comprise flowing a silicon-comprising gas and a conductivity enhancing dopant over the substrate.

76. The method of Claim 75, wherein the conductivity enhancing dopant is flowed at an increasing rate over time to provide a low to high concentration of the dopant within the epitaxial layer.

77. The method of Claim 72, wherein the step of forming the source and drain regions comprises the steps of:

forming a first epitaxial layer of monocrystalline silicon on the substrate adjacent to the gate structure;

forming a layer of an insulative material over the first epitaxial layer;

removing a portion of the insulative layer to expose only a horizontal surface of the first epitaxial layer;

repeating the foregoing steps to form multiple overlying epitaxial layers until the source and drain regions are of a desired height, the epitaxial layers having insulated sidewalls and an uppermost epitaxial layer having an exposed horizontal surface;

doping the uppermost epitaxial layer with a conductivity enhancing dopant by ion implantation; and

forming a layer of an insulative material over the uppermost epitaxial layer.

78. The method of Claim 77, wherein the uppermost epitaxial layer is doped using a fluorine-comprising gas selected from the group consisting of PF_3, PF_5, AsF_5, and $B^{11}F_3$.

79. (amended) A method of forming an elevated source or drain structure on a substrate having a transistor gate disposed thereon, the method comprising the steps of:

selectively growing, while doping, a first epitaxial layer of monocrystalline silicon on the substrate adjacent to the transistor gate;

depositing a layer of an insulative material onto the first epitaxial layer;

removing ~~only the~~a horizontal surface of the insulative layer such that insulative spacers are formed on sidewalls and a horizontal surface of the first epitaxial layer is exposed;

growing additional overlying epitaxial layers according to the foregoing steps until the elevated source or drain structure reaches a desired height; each epitaxial layer having insulated sidewalls;

wherein, upon growing an uppermost epitaxial layer and depositing the insulative layer thereon, no removal step is performed such that the uppermost epitaxial layer comprises ~~insulated~~insulative spacers disposed on the sidewalls and an insulated horizontal surface.

80. The method of Claim 79, wherein during the steps of selectively growing the epitaxial layers, a conductivity enhancing dopant is deposited at an increasing rate over time to provide a low to high concentration of the dopant within the epitaxial layer.

81. (amended) A method of forming an elevated source or drain structure on a substrate having a transistor gate formed thereon,

selectively growing a first epitaxial layer of monocrystalline silicon on the substrate adjacent to the gate, the first epitaxial layer comprising a horizontal surface and sidewalls;

depositing a layer of an insulative material onto the horizontal surface and the sidewalls of the first epitaxial layer;

removing ~~only~~the insulative layer from the horizontal surface of the first epitaxial layer to form insulative ~~layer;~~spacers on the sidewalls;

growing additional overlying epitaxial layers according to the foregoing steps until the elevated source or drain structure reaches a desired height; each epitaxial layer having ~~insulated~~ insulative spacers formed on the sidewalls and an exposed upper surface;

forming an uppermost epitaxial ~~layer having an exposed top surface;~~ layer;

doping the uppermost epitaxial layer with a conductivity enhancing dopant by ion implantation; and

depositing a layer of an insulative material onto the uppermost epitaxial layer.

82. The method of Claim 81, wherein the uppermost epitaxial layer is doped using a fluorine-comprising gas selected from the group consisting of PF_3, PF_5, AsF_5, and $B^{11}F_3$.

83. (amended) A method of forming an elevated transistor in a semiconductive wafer processing comprising the steps of:

providing a semiconductor substrate;

forming a buried drain in the substrate;

forming an elevated gate over the buried drain by the steps of:

forming a first epitaxial layer over the buried drain;

forming an insulative layer over the first epitaxial layer;

removing a portion of the insulative layer to form insulative spacers on sidewalls and expose~~only~~ a horizontal surface of the first epitaxial layer;

forming a second epitaxial layer over the first epitaxial layer;

forming an insulative layer over the second epitaxial layer; and

repeating the foregoing steps to form additional overlying epitaxial layers to form a pillar-like structure having a desired height; each epitaxial layer having ~~insulated sidewalls, and the uppermost epitaxial layer having~~ insulative spacers formed on the sidewalls and an exposed horizontal surface; and

forming a source region onto the gate by forming at least one epitaxial layer over the uppermost epitaxial layer, while doping.

84. The method of Claim 83, wherein the step of forming the buried drain comprises doping an area of the substrate with an n-type dopant.

85. The method of Claim 84, wherein the substrate is doped by ion implantation.

86. The method of Claim 84, wherein the n-type dopant is selected from the group consisting of phosphine, arsine, and combinations thereof.

87. The method of Claim 84, wherein the doped area of the substrate is about 50 nm to about 100 nm wide.

88. The method of Claim 83, wherein the step of forming the source region comprises doping the at least one epitaxial layer with an n-type dopant.

89. (amended) A method of semiconductive wafer processing, comprising forming an elevated transistor by the steps of:

providing a semiconductor substrate;

forming a buried drain in the substrate;

forming an elevated gate over the buried drain, the gate comprising multiple overlying epitaxial layers in a vertical orientation with each epitaxial layer ~~having~~ comprising sidewalls and an upper surface, and insulative spacers formed on the sidewalls; and

forming a source region over the uppermost epitaxial layer of the gate, the source region comprising one or more epitaxial layers, each layer ~~having~~ comprising sidewalls and an upper surface, and insulative spacers formed onto the sidewalls and the uppermost layer having an insulated top surface.

90. (amended) The method of Claim 89, wherein the step of forming the elevated gate comprises:

depositing an epitaxial layer above the buried drain;

depositing a layer of insulative material over the epitaxial layer;

removing a horizontal surface of the insulative layer to expose the epitaxial layer and form insulative spacers on sidewalls of the epitaxial layer; and

repeating the foregoing steps until the gate reaches a desired height.

91. The method of Claim 89, wherein the step of forming the source region comprises:

forming an epitaxial layer onto an exposed horizontal surface of an uppermost epitaxial layer of the gate, while doping with a conductivity enhancing dopant.

92. (amended) The method of Claim 91, wherein the conductivity enhancing dopant is an n-type dopant selected from the group consisting of phosphine, arsine, and combinations thereof.

93. The method of Claim 89, wherein the step of forming the source region comprises:

forming an epitaxial layer over an uppermost epitaxial layer, and doping the epitaxial layer of the gate with a conductivity enhancing dopant.

94. The method of Claim 93, wherein the conductivity enhancing dopant is selected from the group consisting of PF_3, PF_5, AsF_5, and combinations thereof.

95. The method of Claim 89, further comprising, prior to the step of forming the elevated gate, removing an oxide layer from the substrate overlying the buried drain.

96. The method of Claim 89, wherein the step of forming the buried drain in the substrate comprises doping an area of the substrate with a conductivity enhancing dopant by ion implantation.

97. The method of Claim 96, wherein the conductivity enhancing dopant is an n-type dopant selected from the group consisting of phosphine, arsine, and combinations thereof.

98. The method of Claim 96, wherein the doped area of the substrate is about 50 nm to about 100 nm wide.

99. The method of Claim 89, wherein a plurality of elevated transistors are formed on the substrate so as to define an array of transistors.

100. The method of Claim 99, further comprising forming shallow trench isolation regions in the substrate to isolate the transistor.